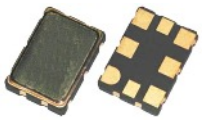
Frequency Switchable Oscillator 15.0MHz to 2,100MHz

FEATURES

- **Four switchable frequencies**
- **Integrated jitter performance of 150fs RMS**
- **CMOS or differential output**



GENERAL SPECIFICATIONS at Ta = +25°C

Output Logic	CMOS	PECL	LVDS	HCSL	CML
Supply Voltage	+1.8V ±5%	--	+1.8V ±5% †	+1.8V ±5%	+1.8V ±5%
	+2.5 V ±10%	+2.5V ±10%	+2.5V ±10%	+2.5V ±10%	+2.5V ±10%
	+3.3 V ±10%	+3.3V ±10%	+3.3V ±10%	+3.3V ±10%	+3.3V ±10%
Available Frequency Range	15MHz ~ 250MHz	15MHz ~ 2,100MHz	15MHz ~ 2,100MHz	15MHz ~ 700MHz	15MHz ~ 2,100MHz
Output Load	15pF	50Ω into Vdd - 2V or Thevenin equivalent	100Ω between output and complementary output	50Ω to GND	50Ω to Vdd
Output Logic 'HIGH' '1'	90% of Vdd min.	Vdd - 1.03V min. Vdd - 0.6V max.	Vdd: 1.4V typ. Vdd: 1.6V max.	Vdd: 0.66V min. Vdd: 1.15V max.	Vdd - 0.085V min. Vdd = Vdd max.
Output Logic 'LOW' '0'	10% of Vdd max.	Vdd - 1.85V min. Vdd - 1.6V max.	Vdd: 1.1V typ. Vdd: 0.9V min.	Vdd: -0.15V min. Vdd: 0.15V max.	Vdd - 0.6V min. Vdd - 0.32V max.
Current Consumption (Vdd = +3.3V)	75mA typ. 90mA max.	100mA typ. 120mA max.	75mA typ. 90mA max.	80mA typ. 100mA max.	70mA typ. 85mA max.
Current With Output Disabled	62mA typ.	99mA typ.	74mA typ.	79mA typ.	69mA typ.
Output Voltage Swing	--	595mV min. 930mV max.	250mV min. 450mV max.	450mV min. 700mV typ.	200mV min. 600mV max.
Rise/Fall Time	5ns max. (10%~90% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max. (20%~80% waveform)	0.4ns max. (20%~80% waveform)

Phase Jitter (12kHz to 20MHz)	156.250MHz: 148 fsec typ.; 312.500MHz: 147 fsec typ.; 644.530MHz: 141 fsec typ.; 2.000MHz: 155 fsec typ.			
Frequency Stability Codes	Frequency Stability over Operating Temp. Range	±25ppm	±50ppm	±100ppm
	Commercial *(-10° to +70°C)*	*A*	*B*	*C*
	Industrial *(-40° to +85°C)*	*D*	*E*	*F*
	Extended Industrial (-40°C to +105°C)	--	*H*	*I*
Duty Cycle	50±5%			
Start-up Time	5.0ms typ., 10.0ms max.			
Ageing at 25°C	±3ppm max for first year			
Storage Temp. Range	-55° to +150°C			

FREQUENCY SELECTION FUNCTION

FS0 Control on Pad 1	70% of Vdd min. to logic level '1'
	30% of Vdd max. to logic level '0'
FS1 Control on Pad 2	70% of Vdd min. to lofic level '1'
	30% of Vdd max. to logic level '0'
Frequency Select Timing: Tfs	10.0msec. max.
Frequency Configurations:	The frequency output 1~4 setting is done based on logic levels in Table 1 below.

† 1.8V LVDS Requires AC coupling (100nF series capacitor)

FS1	FS0	Frequency Output
0	0	Frequency 1
0	1	Frequency 2
1	0	Frequency 3
1	1	Frequency 4

Table 1

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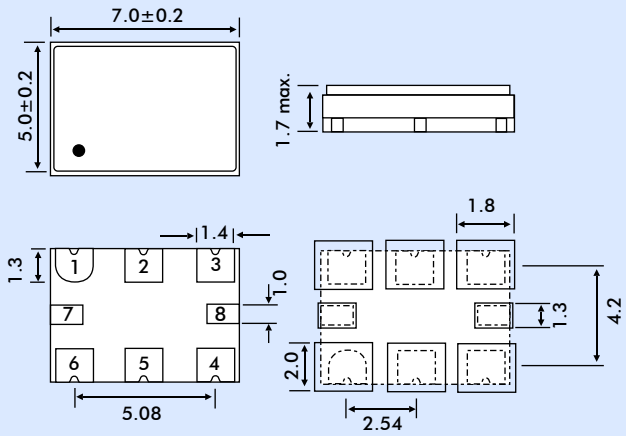
OUTLINE DIMENSIONS (Unit: mm) **SUGGESTED PAD LAYOUT FOR SMDs**

EHCJFN578



Pad Connections

Pad 1: FS0 Control
Pad 2: FS1 Control
Pad 3: Ground
Pad 4: CMOS: Output, Differential: Output
Pad 5: CMOS: NC, Differential: Complementary Output
Pad 6: Supply Voltage
Pads 7, 8: No Connection

PART NUMBER FORMAT AND EXAMPLE

Example: 25 EHCCJFN 578 - E - 120 / 250 / 600 / 1024

Supply Voltage
18 = 1.8 Volts
25 = 2.5 Volts
3 = 3.3 Volts

Output Type
T = CMOS
P = LVPECL
D = LVDS
C = HCSL
Q = CML

Package
578 = 7.0 x 5.0mm

Frequency Stability
See Codes on Page 1

Frequency 1/2/3/4

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