

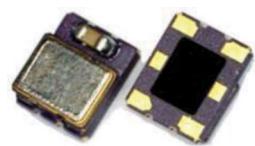
Temperature Compensated Crystal Oscillators [TCXO " M " and VCTCXO " VM "]

TCXO			VCTCXO			N series	SMD	2.5 V	3.3 V	Min.	Max.
MQN _ T	MQN _ P	MQN _ D	VMQN _ T	VMQN _ P	VMQN _ D					10 MHz	1,500 MHz
CMOS	LVPECL	LVDS	CMOS	LVPECL	LVDS						

Features

0.8 pS Phase Jitter (typical)

The (V)MQN326T, (V)MQN326P and (V)MQN326D Series are members of Mercury's Q-Family Temperature Compensated oscillators that can be delivered within days. With low current consumption (44 mA for LVPECL 212.500 MHz at 3.3V) and an integrated phase jitter performance of 0.8 pS RMS, they have gained its precision frequency control market position by providing engineers with few-day samples for prototypes and low cost, fast delivery for volume production .



General specifications , at Ta=+25°C , CL=15pF

Model	(V)MQN326T	(V)MQN326P	(V)MQN326D						
Output Logic	LVCMOS / LVTTL	LVPECL	LVDS						
Supply Voltage V _{DD} (code)	+ 2.5 V _{DD} ± 5% (voltage code " 25 ") + 3.3 V _{DD} ± 5% (voltage code " 33 ")	+ 2.5 V _{DD} ± 5% (voltage code " 25 ") + 3.3 V _{DD} ± 5% (voltage code " 33 ")	+ 2.5 V _{DD} ± 5% (voltage code " 25 ") + 3.3 V _{DD} ± 5% (voltage code " 33 ")						
Available Frequency Range	10 ~ 250 MHz	10 ~ 1,500 MHz	10 ~ 1,500 MHz						
Load	15 pF	50 Ω into Vcc - 2V or Thevenin equivalent	100 Ω						
Output Logic " High " , " 1 "	90 % V _{DD}	V _{DD} - 1.03 (min.), V _{DD} - 0.6 (max.)	1.4 V Typical , 1.6 V max.						
Output Logic " Low " , " 0 "	10 % V _{DD}	V _{DD} - 1.85 (min.), V _{DD} - 1.6 (max.)	1.1 V Typical , 0.9 V min.						
(V _{DD} = + 2.5V)	50 MHz : 24 mA	156 MHz : 36 mA	156 MHz : 22 mA						
Current Consumption	125 MHz : 28 mA	600 MHz : 40 mA	600 MHz : 28 mA						
All values are typical and over the operating temperatures.	200 MHz : 30 mA	800 MHz : 46 mA	800 MHz : 30 mA						
		1,000 MHz : 50 mA	1,000 MHz : 34 mA						
(V _{DD} = + 3.3V)	50 MHz : 26 mA	156 MHz : 40 mA	156 MHz : 25 mA						
Current Consumption	125 MHz : 30mA	600 MHz : 45 mA	600 MHz : 30 mA						
All values are typical and over the operating temperatures.	200 MHz : 34 mA	800 MHz : 48 mA	800 MHz : 32 mA						
		1,000 MHz : 52 mA	1,000 MHz : 36 mA						
Current with Output Disabled	18 mA (typical)	18 mA (typical)	18 mA (typical)						
Rise Time / Fall Time	1.5 nS. (Typical) , 3.0 nS. (max.) Tr / Tf : 10% ↔ 90% waveform	0.2 nS. (Typical) , 0.5 nS. (max.) Tr / Tf : 20% ↔ 80% waveform	0.2 nS. (Typical) , 0.4 nS. (max.) Tr / Tf : 20% ↔ 80% waveform						
Initial Calibration Tolerance	±1.0 ppm. max. at +25°C±2°C. (upon shipment)								
	Temperature (ref to +25°C)	± 2.5 ppm over -30°C to +85°C (default) ± 1.0 ppm over -40°C to +85°C (available)							
Frequency Stability Codes	Aging	± 1.0 ppm max. , per year at 25°C							
	Voltage Change	± 0.2 ppm max. , for a ±5% input voltage change.							
	Load Change	± 0.2 ppm max. , for a ±10% load condition change.							
	Reflow	± 1.0 ppm max. , 1 reflow and measured 24 hours afterwards.							
Duty Cycle	50 % ± 5%								
Start-up Time	5 m sec. (max.)								
Aging at Ta = +25°C	± 2 ppm max. first year at 25°C ; ± 10 ppm max. over 10 years								
Storage Temperature	-55°C to + 150°C								
SSB Phase Noise [dBc / Hz (typical)]	Offset 125 MHz 212.5 MHz 312.5 MHz	10 Hz -51 -42 -49	100 Hz -93 -87 -88	1K Hz -111 -105 -107	10K Hz -123 -115 -111	100K Hz -125 -118 -114	1M Hz -135 -130 -124	10M Hz -155 -151 -147	Phase Jitter (12KHz ~ 20 MHz) 0.73 pS 0.85 pS 0.88 pS

Control Voltage Function on Pad 1

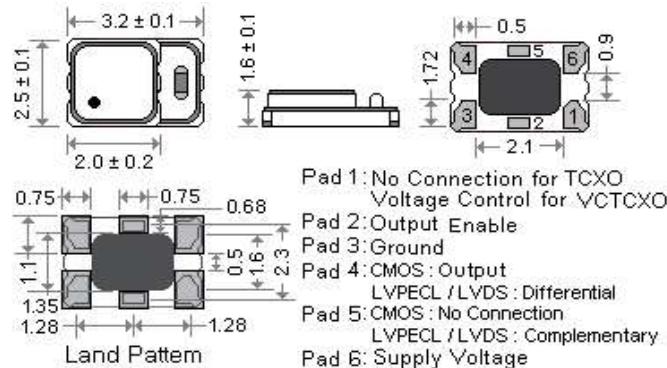
Control Voltage Center and Range	+1.5V ± 1.0V for both V _{DD} = 2.5V and 3.3V
Frequency Pulling Range	± 8 ppm min.
Linearity	± 1 % typical. ± 10% max.
Transfer Function	Positive Transfer
Absolute Voltage	4.0 V max.
Input Impedance	770 KΩ typical.
Harmonics	-5.0 dBc max.

Output Enable Function on pad 2

OE Control on Pad 2	70% of V _{DD} (min.) to enable output. (Open connection prohibit.)
	30% of V _{DD} (max.) to disable output (high impedance).
Output Enable Time / Disable Time	200 nS. Max. / 50 nS. Max.
	0.8 pS typical (12 KHz to 20 MHz)
Integrated Phase Jitter	< 150 fS (1.875 KHz to 20 MHz)

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs

[MQN326T] , [MQN326P] , [MQN326D]



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CMOS	LVPECL	LVDS	CMOS	LVPECL	LVDS						

Part Number Format and Example

Example : VMQN326D33 - 622.080 - 2.0 / -40+85

VMQN	326	D	33	-	622.080	-	2.0	/	-40+85
Hold Type	Package	T : CMOS	Supply Voltage						
" MQN " : TCXO	" 326 "	P : LVPECL	" 33 " for 3.3V						Operating
" VMQN " : VCTCXO	(3.2 * 2.5 mm)	D : LVDS	" 25 " for 2.5V						Temperature Range

Test Circuits and Output Waveforms

