

HPQN --

LVPECL
Differential

0.6 pS
Phase Jitter

SMD

2.5 V

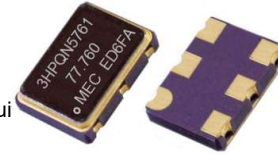
3.3 V

Min.
150 MHz

Max.
1.5 GHz

Features

Low current consumption (54 mA for LVPECL 622.080 MHz at 3.3V) and an integrated phase jitter performance of 0.6 pS RMS. Gaining its precision frequency control market position by providing engineers with few-day samples for prototypes and low cost, fast delivery for volume production. The perfect solution to replace traditional XO's & VCXO's that use a more expensive, highfrequency, fundamental crystal and a noisy PLL multiplier circuit.



General specifications , at Ta=+25°C , CL=15pF

Output Logic		LVPECL Differential				
Model		HPQN				
Package (dimensions) unit : mm		HPQN 3261 (3.2 * 2.5 * 1.0)	HPQN 5361 (5.0 * 3.2 * 1.2)	HPQN 5761 (7.0 * 5.0 * 1.8)		
Supply Voltage V _{DD}		+2.5 V _{DD} ± 5%		+3.3 V _{DD} ± 5%		
Available Frequency Range		150 MHz 1.5 GHz				
Integrated Phase Jitter (12 KHz to 20 MHz)		0.6 ps typical (12 KHz to 20 MHz) < 100 fs (1.875 KHz to 20 MHz)				
Current Consumption		100 MHz : 48 mA max ; 250 MHz : 50 mA max ; 500 MHz : 55 mA max ; 750 MHz : 59 mA max ; 1 GHz : 62 mA max ; 1.35 GHz : 68 mA max				
Rise Time / Fall Time		0.2 ns typical , 0.5 ns max. [20%↔80% of the PECL wave form]				
SSB Phase Noise [dBc / Hz (typical)]		Offset	77.760 MHz (3.3V)	156.250 MHz (3.3V)	622.08 MHz (3.3V)	1250 MHz (3.3V)
		10 Hz	-74	-67	-51	-32
		100 Hz	-104	-92	-77	-68
		1 KHz	-121	-112	-99	-94
		10 KHz	-130	-121	-109	-103
		100 KHz	-134	-124	-114	-105
		1 MHz	-140	-136	-121	-117
Output Logic " High " , " 1 "		V _{DD} - 1.03 min. , V _{DD} - 0.6 max. Termination: R _L =50 Ω to (V _{DD} - 2.0V). See test circuit below.				
Output Logic " Low " , " 0 "		V _{DD} - 1.85 min. , V _{DD} - 1.6 max. Termination: R _L =50 Ω to (V _{DD} - 2.0V). See test circuit below.				
Output Voltage Swing		595 mV min. , 750 mV typ. , 930 mV max.				
Load		50 Ω into V _{cc} - 2V or Thevenin equivalent				
Start-up Time		5.0 ms typical , 10 m sec. (max.)				
Duty Cycle		50% ± 5%				
Storage Temperature		-55°C to + 150°C				
Aging at Ta = +25°C		± 3 ppm max. first year ; ± 2 ppm max. per year thereafter				
Frequency Stability Codes		Frequency Stability over Operating Temperature Range		± 25 ppm	± 50 ppm	± 100 ppm
		Commercial (-10°C to +70°C)		A	B	C
		Industrial (-40°C to +85°C)		D	E	F
OE Function. 5761 on pad 1		Enable	When 70% min. of V _{DD} to Enable Output. Enable time : 200 n sec. (max.)			
		Disable	When 30% max. of V _{DD} to Disable Output. Disable current : 16 mA max. , Disable time : 50 n sec. (max.)			

Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs

HPQN3261	HPQN5361	HPQN5761
<p>3.2 ± 0.1 2.5 ± 0.1 1.0 ± 0.1 0.9 2.4 0.5 0.6 1.2</p> <p>Pad 1 : Tri - state Pad 2 : No Connection Pad 3 : Ground Pad 4 : Output Pad 5 : Complementary Pad 6 : Supply Voltage</p>	<p>5.0 ± 0.2 3.2 ± 0.2 1.2 ± 0.1 0.84 1.2 1.0 2.54 0.64 1.2 2.54</p> <p>Pad 1 : Tri - state Pad 2 : No Connection Pad 3 : Ground Pad 4 : Output Pad 5 : Complementary Pad 6 : Supply Voltage</p>	<p>7.0 ± 0.2 5.0 ± 0.2 1.8 ± 0.1 5.08 2.0 4.2 2.54 1.8 1.4 2.6 5.08</p> <p>pad 1 : Tri - state pad 2 : No connection pad 3 : Ground pad 4 : Output pad 5 : Complementary pad 6 : Supply Voltage</p>

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