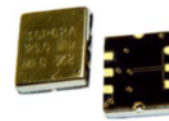


PECL 11.4 x 9.6 x 3.0mm SMD

Page 1 of 2

- Frequency range 38MHz to 640MHz
- LVPECL Output
- Supply Voltage 3.3 VDC
- Integrated Phase Jitter 0.4ps typical



GENERAL SPECIFICATION

Model:	GPF Series
Technology:	High Q fundamental crystal with low jitter multiplier circuit
Output Logic:	LVPECL
Frequency range:	38.0MHz to 640.0MHz
Supply Voltage (V _{DD}):	+3.3V ±5% (Part code = '3')
Output Logic High '1':	V _{DD} -1.025 min.*
Output Logic Low '0':	V _{DD} -1.620 min.*
Integrated Phase Jitter:	0.4ps typical, 0.5ps max. (for 156.250MHz)
Period Jitter RMS:	3ps typical, 5ps max.
Period Jitter Peak to Peak:	20ps typical, 30ps max.
Phase Noise:	See table
Frequency Stability:	See table
Current Consumption	
38MHz to 100MHz:	65mA max.
100MHz to 320MHz:	80mA max.
320MHz to 640MHz:	90mA max.
Rise/Fall Times:	0.55ns max. (from 20% to 80% of PECL wave form)
Start-up Time:	10ms max.
Duty Cycle:	50%±5% measured at V _{DD} -1.3V
Ageing:	±3ppm max. first year, ±2ppm/year thereafter
Control Voltage Centre:	+1.65V, V _{CON} = 0.3V to 3.0V
Frequency Deviation Range:	±80ppm (min.)
Linearity:	6% typical, 10% max.
Slope Polarity:	Positive. Increase of control voltage increases output frequency
Modulation Bandwidth:	25kHz min.
Input Impedance:	60kΩ min.
Enable/Disable:	See below

* Termination: RL = 50Ω to (V_{DD} - 2.0V). See test circuit.

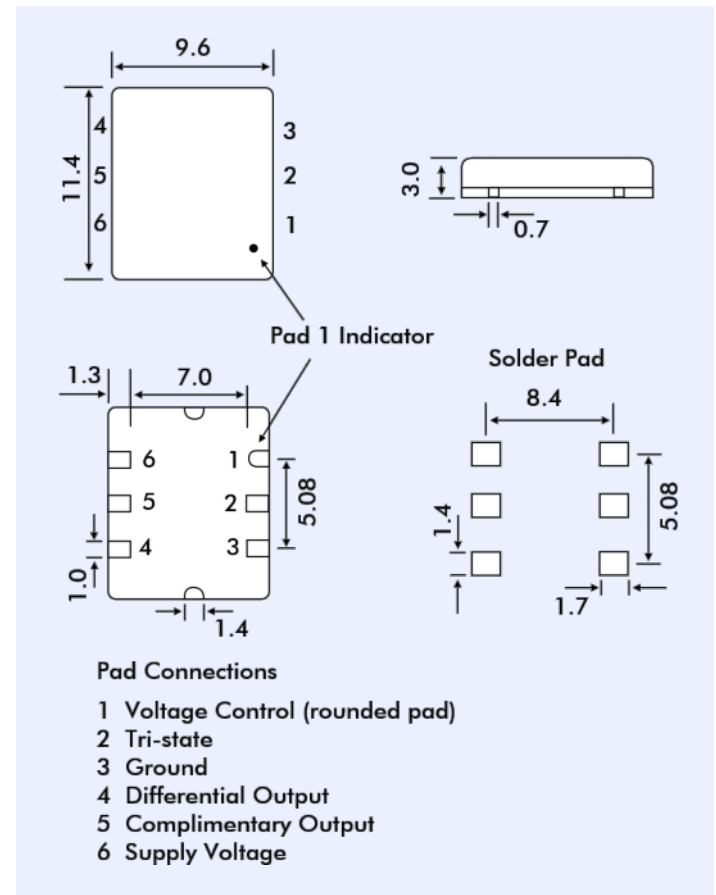
ENABLE/DISABLE FUNCTION (PAD2)

No Connection:	Differential PECL and complimentary PECL outputs enabled.
Disable:	Both outputs are disable (high impedance) when Pad 2 is taken below 0.45V ref to ground. Oscillator is always on, only output buffer stage is disabled.
Enable:	Both outputs are enabled when Pad 2 is take above 1.45V ref to ground.
Enable/Disable Time:	10ns max.

PHASE NOISE at 156.250MHz

Offset	Value
10Hz	-62 dBc/Hz
100Hz	-92 dBc/Hz
1kHz	-120 dBc/Hz
10kHz	-132 dBc/Hz
100kHz	-128 dBc/Hz
1MHz	-140 dBc/Hz
10MHz	-150 dBc/Hz

OUTLINE AND DIMENSIONS



VOLTAGE-CONTROL CHARACTERISTICS

Control Voltage Centre:	+1.65V (V _{CON} = +0.3V to +3.0V)
Frequency Deviation Range:	±80ppm Use 'N' (minimum), 'M' (maximum) or 'T' (typical)
Linearity:	6% typical, 10% maximum
Slope Polarity:	Positive (increase of control voltage increases output frequency)
Modulation Bandwidth:	25kHz min., (-3dB, 0V ≤ V _{control} ≤ 3.3V)

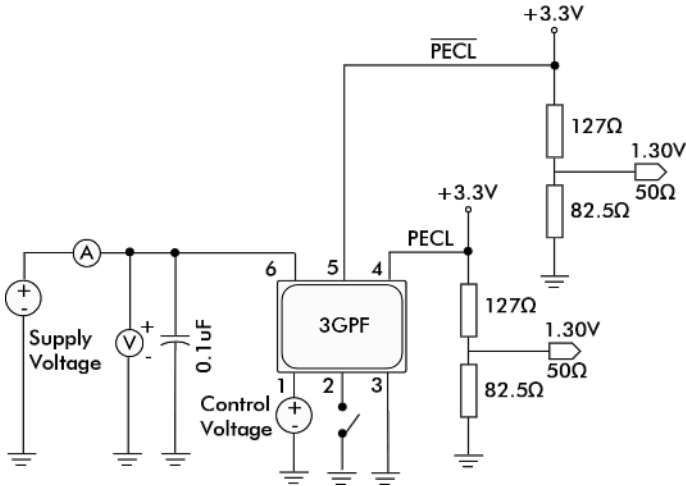
FREQUENCY STABILITY OVER TEMPERATURE

Frequency Stability over Operating Temp. Range*	±25ppm	±50ppm	±100ppm
Commercial -10° to +70°C	A	B	C
Industrial -40 to +85°C	D	E	F

* If non-standard temperature stability is required enter the desired stability in ppm after either 'C' (-10° to +70°) or 'I' (-40° to +85°C) Example: 'C20' = ±20ppm over -10 to +70°C

PECL 11.4 x 9.6 x 3.0mm SMD

PECL VCXO TEST CIRCUIT



PART NUMBER SCHEDULE

Example: 3GPF63 B -100N -155.520

Supply Voltage +3.3V

Series Designator GPF63

Add 'G' here for RoHS compliance

Stability over Temperature Range

A = ±25ppm over -10° to +60°C

B = ±50ppm over -10° to +60°C

C = ±100ppm over -10° to +60°C

D = ±25ppm over -40° to +85°C

E = ±50ppm over -40° to +85°C

F = ±100ppm over -40° to +85°C

Pullability in ±ppm

Pullability Determinator

N = minimum

M = maximum

T = Typical

Frequency in MHz