11.4 x 9.6 x 3.0mm 4 pad SMD CMOS

- **Frequency range 0.625MHz to 50.0MHz**
- **CMOS/TTL Output**
- **Supply Voltage 5.0 V or 3.3 VDC**
- **Integrated Phase Jitter 1ps typical**
- **Low cost unit**

RoHS

SUPPLY VOLTAGE DEPENDENT SPECIFICATION

Model:	'G' Series	
Input Voltage:	Vdd = +3.3VDC±5%	Vdd = +5.0VDC±10%
Frequency Range*:	0.625MHz ~ 50.0MHz	1.0MHz ~ 50.0MHz
Output Wave Form:	CMOS/TTL	
Initial Freq. Accuracy	Tune with Vc = 1.65V±0.2V	Tune with Vc = 2.5V±0.2V
Output Logic High '1'	90% Vdd min.	
Output Logic Low '0'	10% Vdd max.	
Frequency Deviation Range:	Standard ±80ppm min.	Standard ±80ppm min.**
Control Voltage Centre:	1.65 VDC	2.5 VDC
Control Voltage Range:	0.3V to 3.0V	0.5V to 1.5V

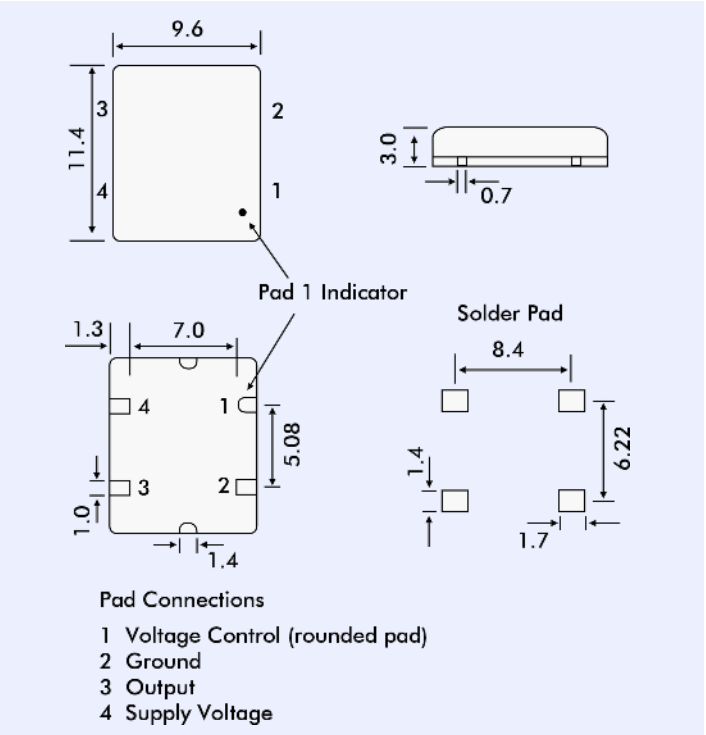
** 'G' series VCXOs use fundamental mode crystals throughout the frequency range*
*** ±200ppm pull range is available with 5.0 Volt supply 'G' series VCXOs*

GENERAL SPECIFICATION

Frequency Stability:		*See table*
Output Load		
	TTL:	2 TTL gates
	CMOS:	15pF
Rise/Fall Times		
	TTL:	6ns max., 4ns typical Measured between 0.4V to 2.4V
	CMOS:	6ns max., 4ns typical Measured between 20% to 80% of wave form, (CL = 15pF)
Duty Cycle:		50%±10% standard, 50%±5% is available, add 'S' to part number
Integrated Phase Jitter:		1ps max. (12kHz to 20MHz)
Period Jitter RMS:		2.0ps typical
Period Jitter Peak to Peak:		14ps max.
Start-up Time:		10ms max., 5ms typical
Current Consumption***:		Frequency dependant (*See note*)
Linearity:		6% typical, 10% max.
Modulation Bandwidth:		10kHz min. Measured at -3dB with V control at 1.65V or 2.5V
Input Impedance:		1MΩ typical
Slope Polarity:		Monotonic and positive (An increase of control voltage increases output frequency.)
Ageing:		±5ppm per year max.

**** Current consumption is frequency dependent, e.g. at 27MHz = 10mA typical with supply voltage 3.3V, and 20mA typical with supply voltage = 5.0V.*

OUTLINE AND DIMENSIONS



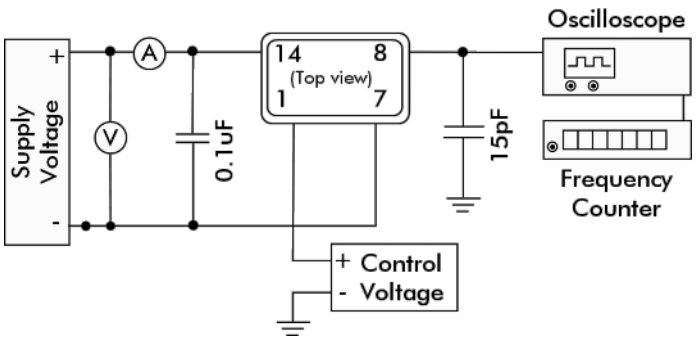
FREQUENCY STABILITY OVER TEMPERATURE

Frequency Stability over Operating Temp. Range*	±25ppm	±50ppm	±100ppm
Commercial -10° to +70°C	A	B	C
Industrial -40 to +85°C	D	E	F

** If non-standard temperature stability is required enter the desired stability in ppm after either 'C' (-10° to +70°) or 'I' (-40° to +85°C) Example: 'C20' = ±20ppm over -10 to +70°C*

11.4 x 9.6 x 3.0mm 4 pad SMD CMOS

CMOS/TTL TEST CIRCUIT



PART NUMBER SCHEDULE

Example: 3G43B-80N-27.000

Supply Voltage
- 3 = +3.3V
- 5 = +5.0 V

Series Designator
- G43

(Add 'G' after Series desgnator for RoHS Compliance)

Stability over temperature range
- A = ±25ppm over -10° to +60°C
- B = ±50ppm over -10° to +60°C
- C = ±100ppm over -10° to +60°C
- D = ±25ppm over -40° to +85°C
- E = ±50ppm over -40° to +85°C
- F = ±100ppm over -40° to +85°C

Pullability in ±ppm

Pullability determinator
- N = minimum
- M = maximum
- T = Typical

Frequency in MHz

TRANSFER FUNCTION

Typical response of 5G14-C-150N-27.000
(at 25°C, positive transfer)